FIG.1

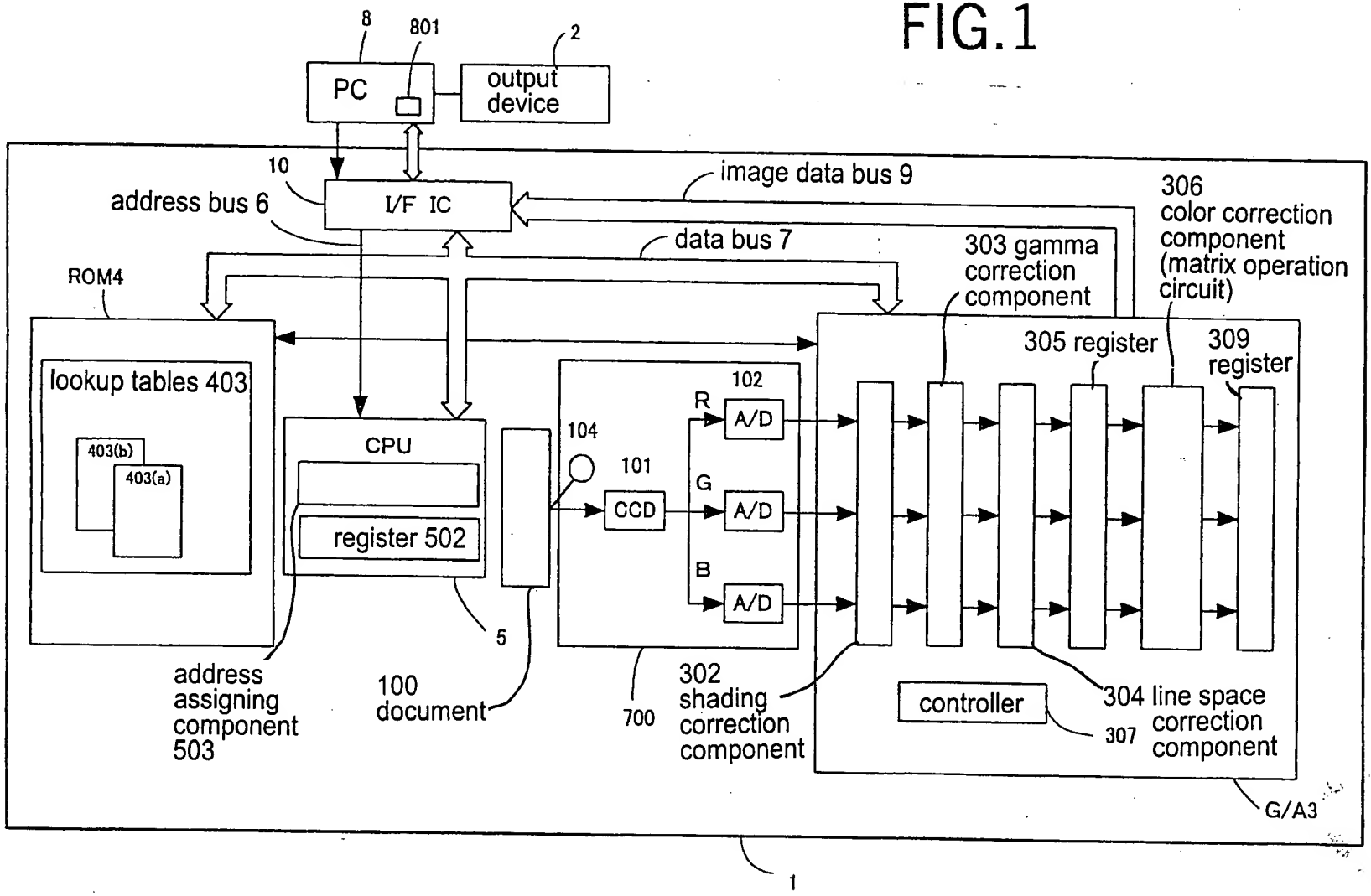

8
801
2
PC
output device
10
address bus 6
I/F IC
image data bus 9
306
color correction component (matrix operation circuit)
data bus 7
303 gamma correction component
ROM4
lookup tables 403
403(b)
403(a)
CPU
register 502
305 register
309 register
102
R
A/D
104
101
CCD
G
A/D
B
A/D
5
address assigning component 503
100 document
700
302 shading correction component
controller
307
304 line space correction component
G/A3
1

FIG.2

lookup tables 403

color lookup table 403(a)

matrix	memory		address
A 1 $\begin{pmatrix} K_{11} & K_{12} & K_{13} \\ K_{21} & K_{22} & K_{23} \\ K_{31} & K_{32} & K_{33} \end{pmatrix}$	R 1	K_{11}	0 H
		K_{21}	1 H
		K_{31}	2 H
	G 1	K_{12}	3 H
		K_{22}	4 H
		K_{32}	5 H
	B 1	K_{13}	6 H
		K_{23}	7 H
		K_{33}	8 H
A 2 $\begin{pmatrix} N_{11} & N_{12} & N_{13} \\ N_{21} & N_{22} & N_{23} \\ N_{31} & N_{32} & N_{33} \end{pmatrix}$	R 1	N_{11}	A H
		N_{21}	B H
		N_{31}	C H
	G 1	N_{12}	D H
		N_{22}	E H
		N_{32}	F H
	B 1	N_{13}	10H
		N_{23}	·
		N_{33}	·
·	·	·	·

monotone lookup table 403(b)

matrix	memory		address
Y 1	R 1	N_{11}	0 H
		N_{21}	1 H
		N_{31}	2 H
	G 1	N_{12}	3 H
		N_{22}	4 H
		N_{32}	5 H
	B 1	N_{13}	6 H
		N_{23}	7 H
		N_{33}	8 H
Y 2	R 2	·	·
·	·	·	·
·	·	·	·
·	·	·	·
·	·	·	·

FIG.3

register 502

memory	matrix		address
A 1 $\begin{pmatrix} K_{11} & K_{12} & K_{13} \\ K_{21} & K_{22} & K_{23} \\ K_{31} & K_{32} & K_{33} \end{pmatrix}$	R 1	K_{11} (K_{11})	0 H
		K_{21} (K_{31})	1 H
		K_{31} (K_{21})	2 H
A 1´ $\begin{pmatrix} K_{11} & K_{12} & K_{13} \\ K_{31} & K_{32} & K_{33} \\ K_{21} & K_{22} & K_{23} \end{pmatrix}$	G 1	K_{12} (K_{12})	3 H
		K_{22} (K_{32})	4 H
		K_{32} (K_{22})	5 H
	B 1	K_{13} (K_{13})	6 H
		K_{23} (K_{33})	7 H
		K_{33} (K_{23})	8 H

FIG.4

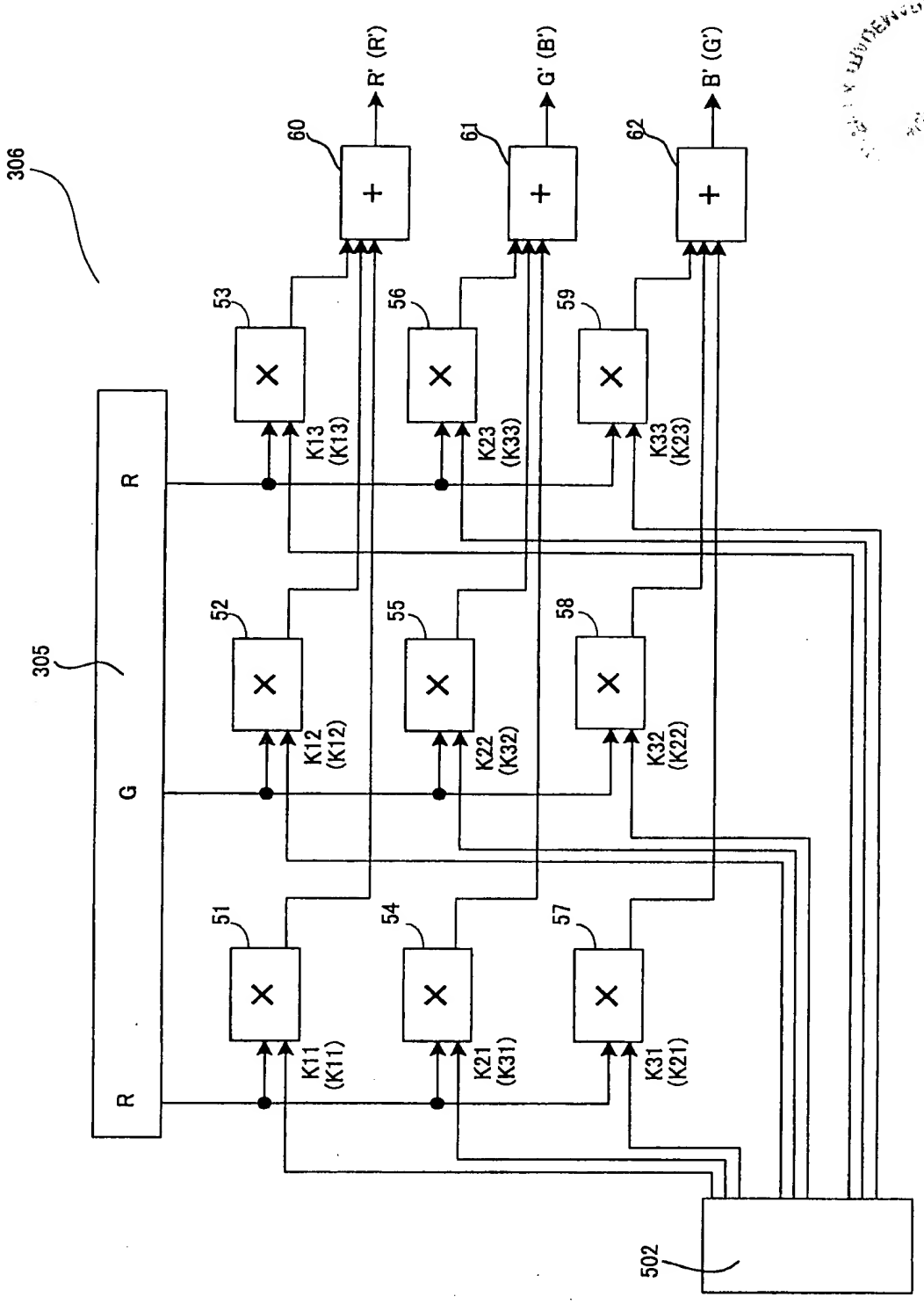

306
305
R
G
R
51
52
53
54
55
56
57
58
59
60
61
62
K11 (K11)
K12 (K12)
K13 (K13)
K21 (K31)
K22 (K32)
K23 (K33)
K31 (K21)
K32 (K22)
K33 (K23)
+
R' (R')
G' (B')
B' (G')
502

FIG.5

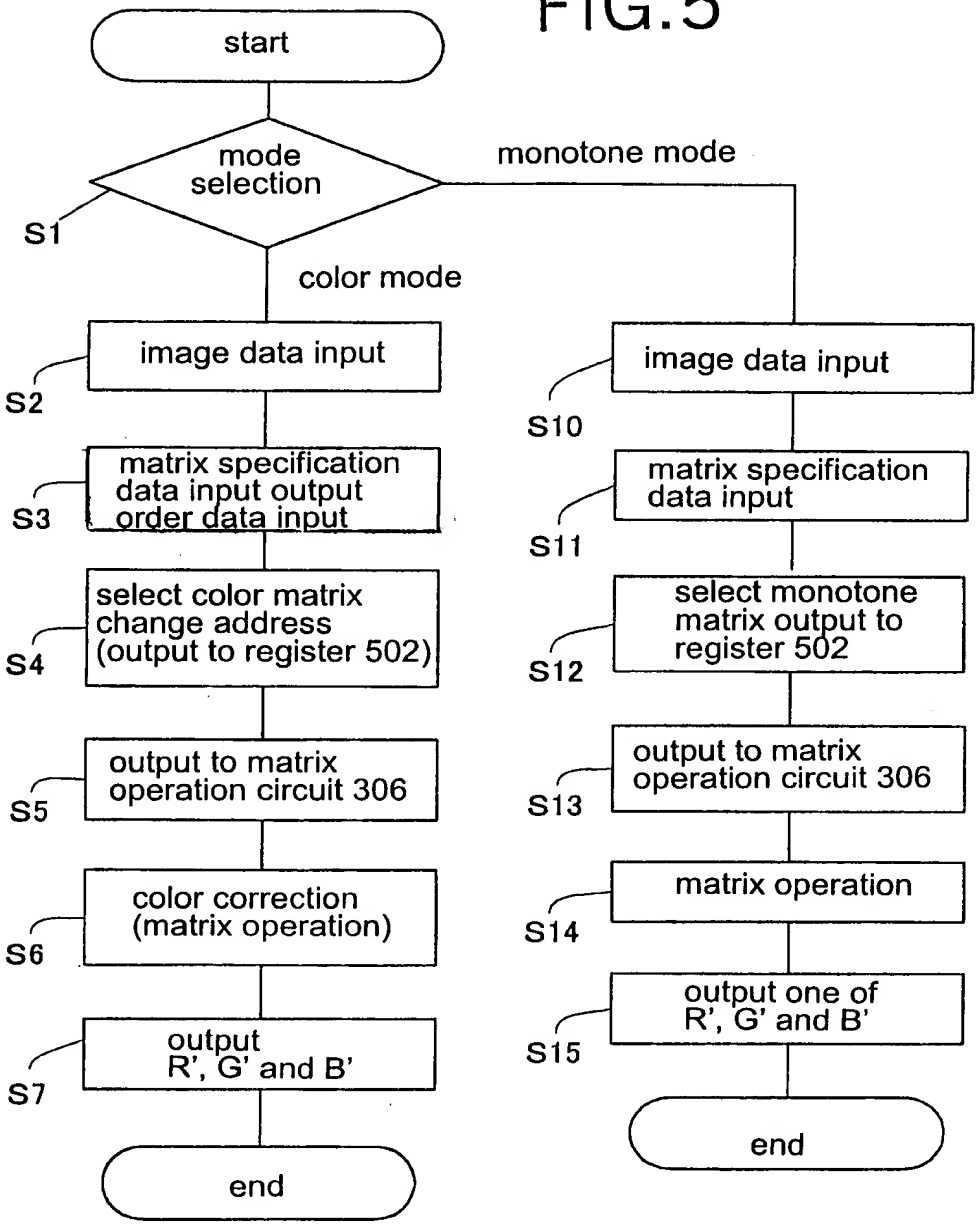

start
mode selection
S1
monotone mode
color mode
image data input
S2
matrix specification data input output order data input
S3
select color matrix change address (output to register 502)
S4
output to matrix operation circuit 306
S5
color correction (matrix operation)
S6
output R', G' and B'
S7
end
image data input
S10
matrix specification data input
S11
select monotone matrix output to register 502
S12
output to matrix operation circuit 306
S13
matrix operation
S14
output one of R', G' and B'
S15
end

FIG.6

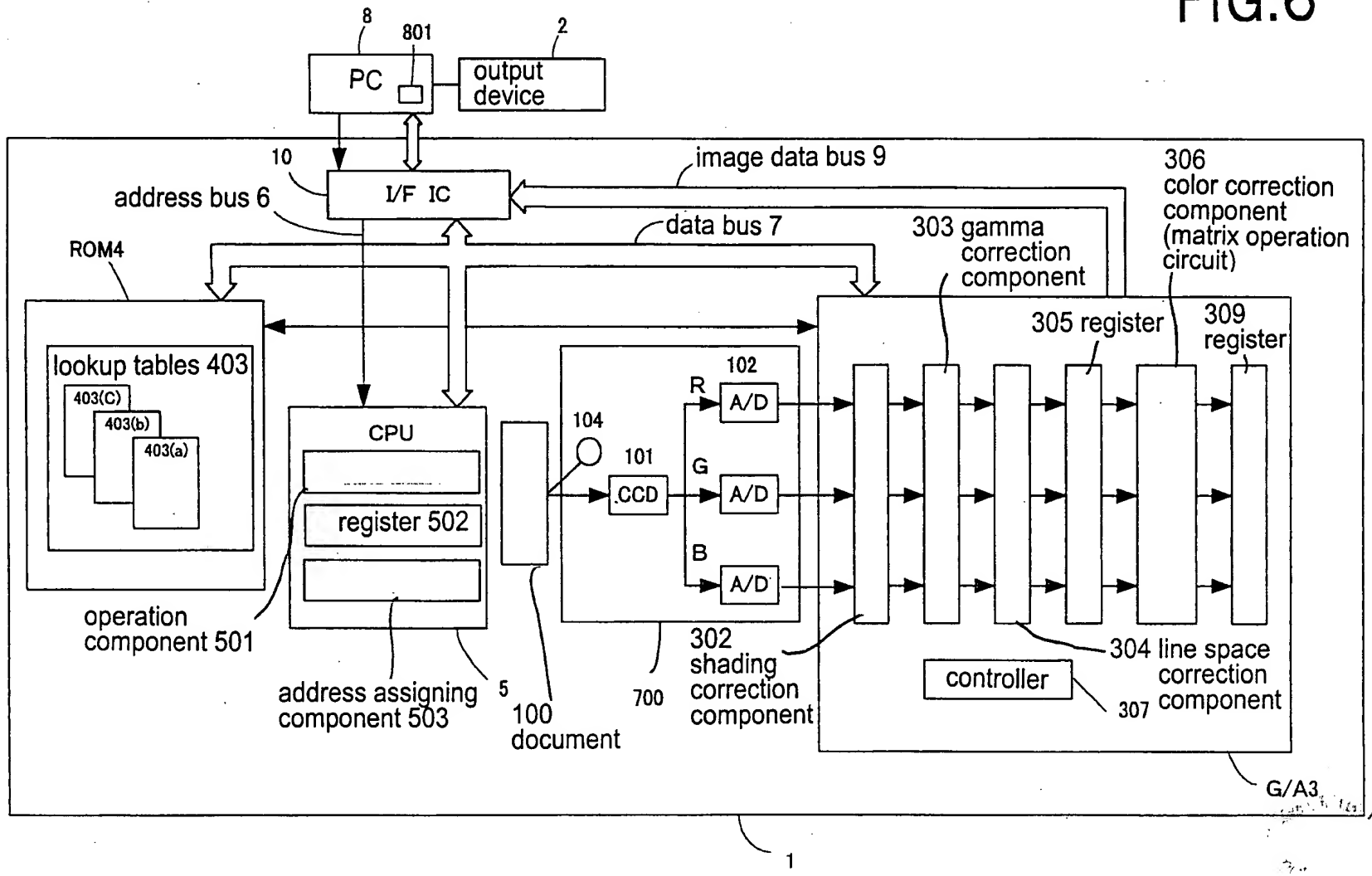
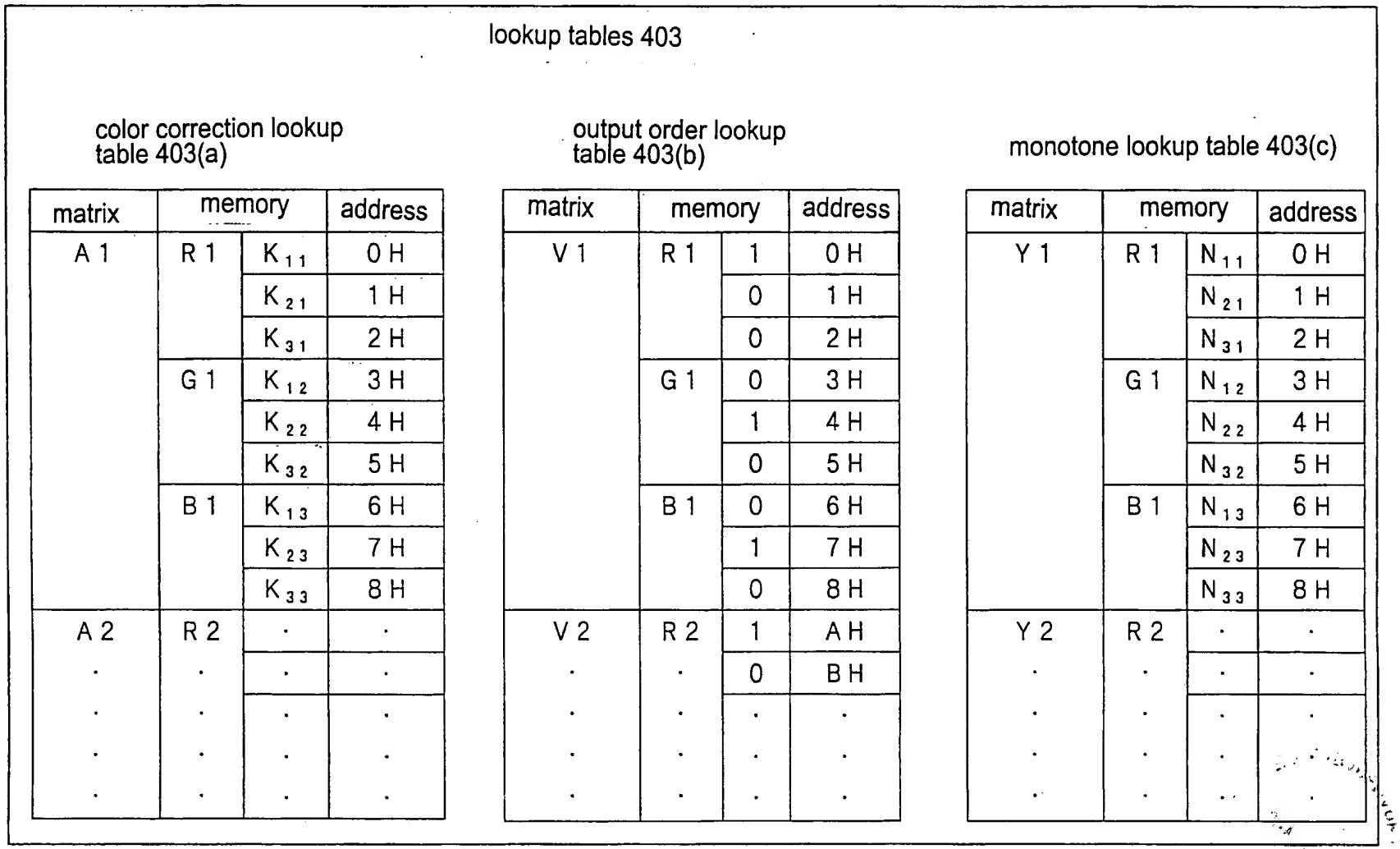

8
801
2
PC
output device
10
I/F IC
address bus 6
image data bus 9
data bus 7
306
color correction component (matrix operation circuit)
303 gamma correction component
ROM4
lookup tables 403
403(C)
403(b)
403(a)
CPU
register 502
operation component 501
address assigning component 503
5
100
document
104
101
CCD
102
R
G
B
A/D
A/D
A/D
700
302
shading correction component
305 register
309 register
304 line space correction component
controller
307
G/A3
1

FIG.7



color correction lookup table 403(a)

matrix	memory		address
A 1	R 1	K_{11}	0 H
		K_{21}	1 H
		K_{31}	2 H
	G 1	K_{12}	3 H
		K_{22}	4 H
		K_{32}	5 H
	B 1	K_{13}	6 H
		K_{23}	7 H
		K_{33}	8 H
A 2	R 2	·	·
·	·	·	·
·	·	·	·
·	·	·	·
·	·	·	·

output order lookup table 403(b)

matrix	memory		address
V 1	R 1	1	0 H
		0	1 H
		0	2 H
	G 1	0	3 H
		1	4 H
		0	5 H
	B 1	0	6 H
		1	7 H
		0	8 H
V 2	R 2	1	A H
·	·	0	B H
·	·	·	·
·	·	·	·
·	·	·	·

monotone lookup table 403(c)

matrix	memory		address
Y 1	R 1	N_{11}	0 H
		N_{21}	1 H
		N_{31}	2 H
	G 1	N_{12}	3 H
		N_{22}	4 H
		N_{32}	5 H
	B 1	N_{13}	6 H
		N_{23}	7 H
		N_{33}	8 H
Y 2	R 2	·	·
·	·	·	·
·	·	·	·
·	·	·	·
·	·	·	·

FIG.8A

$$\begin{pmatrix} R \\ G \\ B \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} R \\ G \\ B \end{pmatrix} \quad V1$$

FIG.8B

$$\begin{pmatrix} R \\ B \\ G \end{pmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} R \\ G \\ B \end{pmatrix} \quad V2$$

FIG.8C

$$\begin{pmatrix} G \\ R \\ B \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} R \\ G \\ B \end{pmatrix} \quad V3$$

FIG.8D

$$\begin{pmatrix} G \\ B \\ R \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{pmatrix} \begin{pmatrix} R \\ G \\ B \end{pmatrix} \quad V4$$

FIG.8E

$$V5 \quad \begin{pmatrix} B \\ G \\ R \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{pmatrix} \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

FIG.8F

$$V6 \quad \begin{pmatrix} B \\ R \\ G \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix} \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

FIG.9

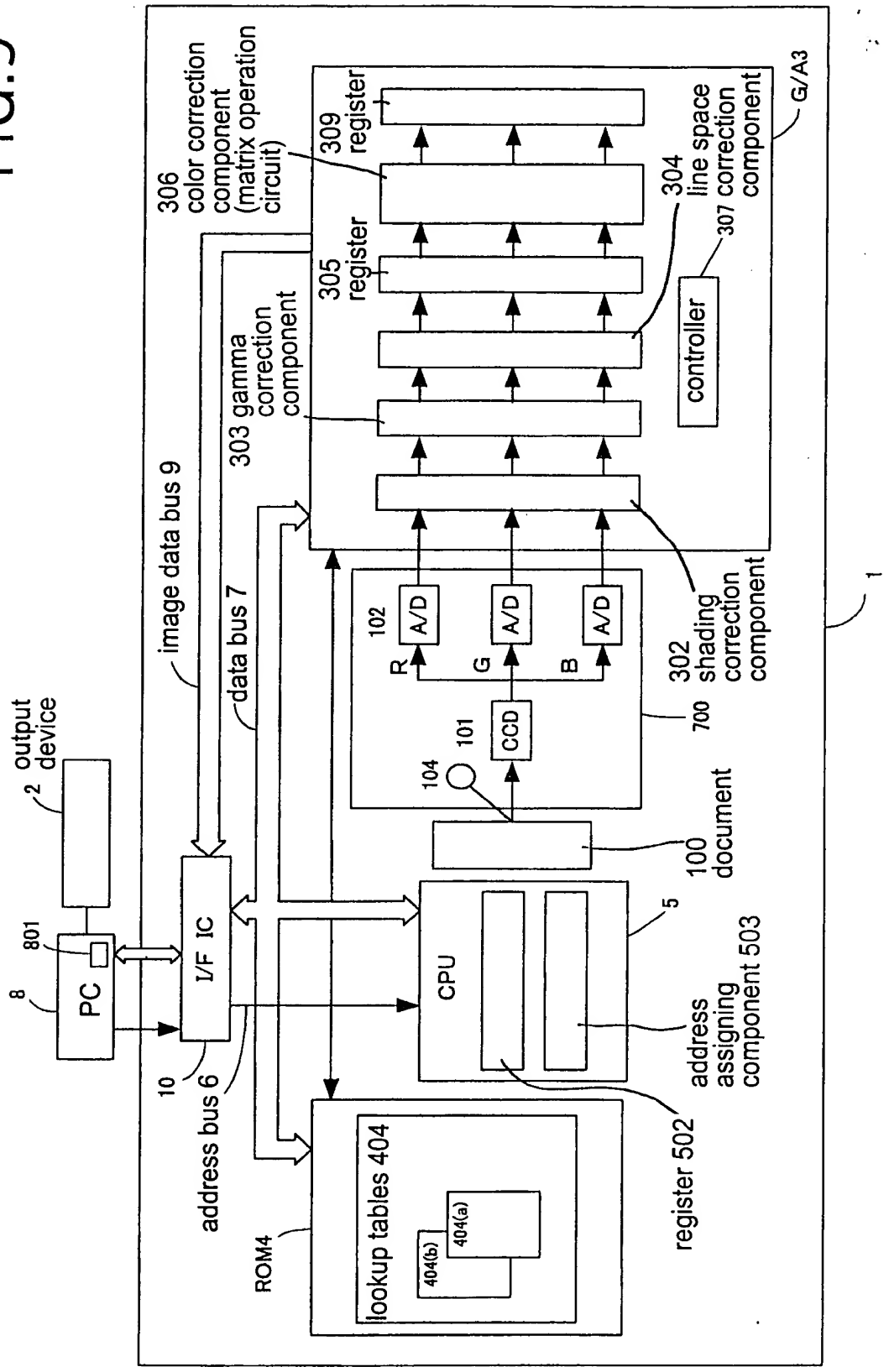

output device
2
801
8
PC
I/F IC
10
address bus 6
image data bus 9
data bus 7
306 color correction component (matrix operation circuit)
303 gamma correction component
305 register
309 register
304 line space correction component
307 controller
G/A3
302 shading correction component
700
102
A/D
R
G
B
101
CCD
104
100 document
1
5
CPU
address assigning component 503
register 502
ROM4
lookup tables 404
404(a)
404(b)

FIG.10

lookup tables 404

combined matrix C (color mode) lookup table 404(a)

matrix	memory		address
C 1	R 1	K_{11}	0 H
		K_{21}	1 H
		K_{31}	2 H
	G 1	K_{12}	3 H
		K_{22}	4 H
		K_{32}	5 H
	B 1	K_{13}	6 H
		K_{23}	7 H
		K_{33}	8 H
C 2	R 2	·	·
·	·	·	·
·	·	·	·
·	·	·	·
·	·	·	·

combined matrix D (monotone mode) lookup table 404(b)

matrix	memory		address
D 1	R 1	M_{11}	0 H
		M_{21}	1 H
		M_{31}	2 H
	G 1	M_{12}	3 H
		M_{22}	4 H
		M_{32}	5 H
	B 1	M_{13}	6 H
		M_{23}	7 H
		M_{33}	8 H
D 2	R 2	·	·
·	·	·	·
·	·	·	·
·	·	·	·
·	·	·	·

PRIOR ART FIG.11